

# Digitally Programmable Delay Units

**SERIES: PDU-1364F  
(6-Bit) TTL Interfaced**



**Features:**

- Input & output TTL buffered
- 6-BIT TTL programmable delay line
- Two (2) separate outputs; inverting & non-inverting
- Completely interfaced
- Compact & low profile

- Temperature coefficient: 100 PPM/°C.

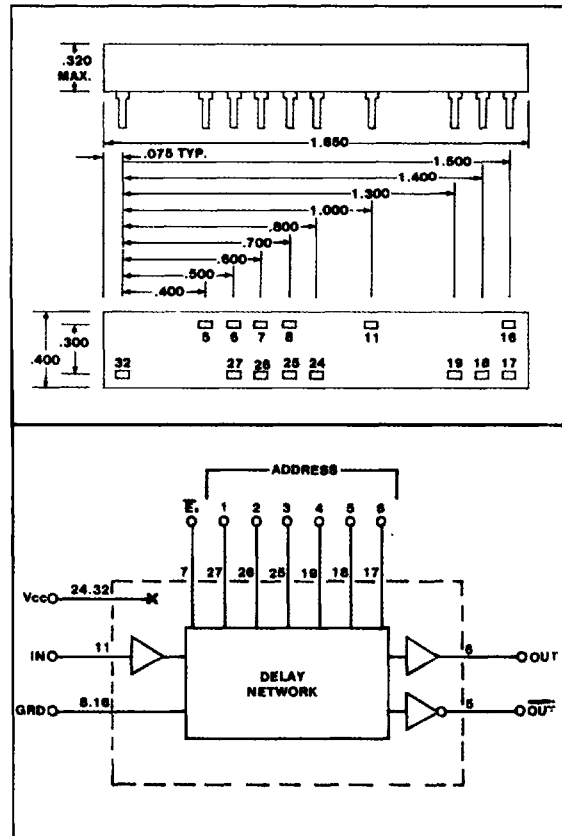
**Test Conditions:**

- Input pulse-width:  $\geq 150\%$  of Max. delay.
- Input pulse spacing:  $\geq 3$  times of Max. delay.
- Input pulse voltage: TTL logic.
- Measurements taken @  $T_a = 25^\circ\text{C}$ ;  $V_{cc} = 5\text{V}$ .



**Specifications:**

- Propagation delay:  
Address to output ( $T_{sua}$ ) = 12 ns typ.  
Enable to output ( $T_{sue}$ ) = 12 ns typ.
- Delay variation: Monotonic in one direction.
- Programmed delay tolerance:  $\pm 5\%$  or 2 ns whichever is greater.
- Inherent delay ( $T_{00}$ ):  
12 ns on pin 5 typical  
11 ns on pin 6 for PDU-1364F-1 thru -10.  
greater for rest of Part Numbers.
- Power dissipation: 850 mw max.
- Supply voltage: 5 Vdc  $\pm 5\%$ .
- Operating temperature: 0-70°C.
- DC parameters: See TTL-Fast Schottky Logic Table on Page 6.



TRUTH TABLE

Enable ( $E_0$ )	Address						Delay Out
	6	5	4	3	2	1	
0	0	0	0	0	0	0	$T_0$
0	0	0	0	0	0	1	$T_1$
0	0	0	0	0	1	0	$T_2$
0	0	0	0	0	1	1	$T_3$
0	0	0	0	1	0	0	$T_4$
0	0	0	0	1	0	1	$T_5$
0	0	0	1	1	1	0	$T_6$
0	0	0	1	1	1	1	$T_7$
0	0	0	1	0	0	0	$T_8$
0	0	0	1	1	1	1	$T_{15}$
0	0	1	0	0	0	0	$T_{16}$
0	0	1	1	1	1	1	$T_{31}$
0	1	0	0	0	0	0	$T_{32}$
0	1	1	1	1	1	1	$T_{63}$
1	0	0	0	0	0	0	1

0 Logic 0 1 Logic 1 0 Don't care.  
 $T_0$  Reference or inherent delay of unit.  
 $T_1$   $T_{63}$  Multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-1364F-0.5	0.5 $\pm$ 0.3	31.5
PDU-1364F-1	1 $\pm$ 0.5	63
PDU-1364F-2	2 $\pm$ 0.5	126
PDU-1364F-3	3 $\pm$ 1.0	189
PDU-1364F-4	4 $\pm$ 1.0	252
PDU-1364F-5	5 $\pm$ 1.0	315
PDU-1364F-6	6 $\pm$ 1.0	378
PDU-1364F-8	8 $\pm$ 1.0	504
PDU-1364F-10	10 $\pm$ 1.5	630